Remarks

Applicants respectfully request reconsideration of this application as amended. Claims 1, 3, 5 and 7 have been amended. Claims 2, 4, 9-22 and 28-34 have been cancelled without prejudice. Claims 35-48 have been added. Therefore, claims 1, 3, 5-8, 23-27 and 35-48 are presented for examination.

Double Patenting

Claims 1-8 and 22-34 stand rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-16 of Jassowski et al., U.S. Patent No. 6,784,558 ("Jassowski").

Applicants herein submit a terminal disclaimer to overcome the double patenting rejection, and respectfully request that the rejection to the claims be withdrawn.

35 U.S.C. §102 Rejections

Claims 1-6 and 28 stand rejected under 35 U.S.C. §102(e) as being clearly anticipated by Hiraga, U.S. Patent No. 6,091,089 ("Hiraga").

Hiraga discloses "[a] semiconductor integrated circuit device [that] has a semiconductor chip, on which are formed a plurality of input/output circuits and input/output pads individually connected." (Abstract, lines 1-4). Hiraga further discloses that "*input/output pads 5 [are] connected to the input/output circuits . . . arranged in a single row*" (col. 4, lines 4-6; emphasis provided) and the single row is "*the innermost row.*" (col. 4, lines 35-36; emphasis provided). Hiraga further discloses that ". . . *input/output pads 6*

and 7 are arranged in a staggered arrangement on both sides of a row of input/output circuits." (col. 4, lines 64-66; emphasis provided).

Claim 1, in pertinent part, recites "a plurality of bond pads configured in a staggered array between the first edge and the core, wherein the staggered array includes an inner ring and an outer ring of bond pads." (emphasis provided). The Examiner has indicated in an Office Action mailed, March 22, 2005 (the "Office Action") that ". . . Hiraga teaches the plurality of bond pads are configured in a staggered array including an inner ring [5] and an outer ring [6] of bond pads." Applicants respectfully disagree with the Examiner's characterization of Hiraga. In contrast, Hiraga teaches that input/output pads 6 and 7 are the pads in the staggered arrangement and not pads 5 and 6. (col. 4, lines 64-66). Nowhere in Hiraga is it taught or reasonably suggested that input/output pads 5 and 6 are in a staggered arrangement. Accordingly, Hiraga does not teach or reasonably suggest "a plurality of bond pads configured in a staggered array between the first edge and the core, wherein the staggered array includes an inner ring and an outer ring of bond pads", as recited by claim 1. (emphasis provided). Applicants respectfully request the withdrawal of the rejection of claim 1 and its dependant claims.

Claims 1 and 2 stand rejected under 35 U.S.C. §102(b) as being clearly anticipated by Hayashi et al., U.S. Patent No. 5,581,109 ("Hayashi").

Hayashi discloses "[a] semiconductor device [that] includes a semiconductor chip, [and] an I/O-cell circuit having a transistor-array part. The semiconductor device further includes a first group of bonding pads and a second group of bonding pads." (Abstract, lines 1-4).

In contrast, claim 1, in pertinent part, recites "a plurality of bond pads configured in a staggered array between the first edge and the core, wherein the staggered array includes an inner ring and an outer ring of bond pads." (emphasis provided). However, nowhere in Hayashi is such a feature taught or reasonably suggested. Accordingly, Applicants respectfully request the withdrawal of the rejection of claim 1 and its dependant claims.

Claims 1 and 2 stand rejected under 35 U.S.C. §102(b) as being clearly anticipated by Pendse et al., U.S. Patent No. 5,818,114 ("Pendse").

Pendse discloses an ". . . I/O pad structure and layout methodology . . ." in which ". . . *the pad layout . . . entails the use of two rows of pads* on the chip periphery as opposed to the more conventional single row. . . arrangement." (Abstract, lines 1-7; emphasis provided).

In contrast, claim 1, in pertinent part, recites "a plurality of bond pads configured in a staggered array between the first edge and the core, wherein the staggered array includes an inner ring and an outer ring of bond pads." (emphasis provided). However, nowhere in Pendse is such a feature taught or reasonably suggested. Accordingly, Applicants respectfully request the withdrawal of the rejection of claim 1 and its dependant claims.

35 U.S.C. §103 Rejections

Claims 7, 8, 22-27, 30 and 34 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Hiraga.

With regard to claims 7, 8, 22-27, 30 and 34, they depend from independent claims 1 and thus, include the limitations of claim 1. Accordingly, Applicants respectfully request the withdrawal of the rejection of claims 7, 8, 22-27, 30 and 34.

Claims 3-8 and 22-24 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Hayashi.

Claim 1, in pertinent part, recites "a plurality of bond pads configured in a staggered array between the first edge and the core, wherein the staggered array includes an inner ring and an outer ring of bond pads." (emphasis provided). Hayashi discloses that "FIG. 10 shows a modified configuration of the semiconductor device . . . in which the bonding pads are *arranged in a form of two lines*." (col. 9, lines 59-63; emphasis provided). Applicants respectfully disagree with the Examiner's assertion the bonding pads in figure 10 of Hayashi are a staggered array including an inner and an outer ring of bond pads. (the Office Action, page 6, lines 13-14). Two lines of bonding pads is not the same as having an inner and outer ring of bonding pads, as recited by claim 1. Additionally, Hayashi would have been motivated to modify the two lines of bonding pads to form an inner and outer ring. This is because Hayashi states that the problem to be fixed is the "*size-increasing of the semiconductor device*" and the way to solve this problem is for ". . . *the bonding pads to be arranged in a plural number of lines* outside the I/O cell circuits", and not in inner and outer rings. (col. 2, lines 1-8; emphasis provided) Accordingly, Applicants respectfully submit that claim 1 and its dependant claims are patentable over Hayashi.

Claims 3-8 and 22-24 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Pendse.

Claim 1, in pertinent part, recites "a plurality of bond pads configured in a staggered array between the first edge and the core, wherein the staggered array includes an inner ring and an outer ring of bond pads." (emphasis provided). Pendse discloses that "FIG. 3 shows a top view of the bonding pad configuration . . . *for a pad ring*." (col. 3, lines 50-51;

emphasis provided). Hence, Pendse does not teach or reasonably suggest a staggered array includes an inner ring and an outer ring of bond pads, as recited by claim 1. There is no motivation in Pendse, based on the single ring structure in figure 3, to add a second pad ring. (col. 3, lines 46-61 and figure 3). Accordingly, Applicants respectfully submit that claim 1 and its dependant claims are patentable over Pendse.

New Claims

New independent claim 35 recites, in pertinent part, "a plurality of conductive interconnects to couple each of the plurality of pre-driver cells to one of the first and second pluralities of driver cells, wherein at least one conductive interconnects is disposed on a layer other than a layer where the plurality of bond pads are disposed." The Examiner has indicated in the Office Action that Hiraga, Hayashi and Pendse all fail to teach wherein at least one conductive interconnect is disposed on a layer other than a layer where the bond pads are disposed. (the Office Action, pages 8, lines 8-9; see also pages 12 and 14). The Examiner further indicated in the Office Action that ". . . the disposing of the conductive interconnect on a different layer is an obvious matter of design choice." (the Office Action, pages 8, lines 9-10). Applicants respectfully disagree with the Examiner's conclusion that "at least one conductive interconnects is disposed on a layer other than a layer where the plurality of bond pads are disposed" is a design choice. (see claim 35). The above limitation adds increased functionality. For example, the Specification states that "[b]ecause the electrically conductive paths between the pre-driver cells . . . and the driver/ESD cells . . . are relatively narrow, . . . the electrically conductive paths may be routed underneath the

bond pads without creating an additional risk of cracking inter layer dielectric material during installation of bond wires." (Specification, page 6, lines 12-17; emphasis provided).

Accordingly, Applicants respectfully submit that claim 35 and its dependant claims 36-43 are distinguished over the cited references.

New independent claim 44 contains similar limitations to those of claim 1. Claims 45-48 depend from claim 44. Accordingly, Applicants respectfully submit that claims 44-48 are distinguished over the cited references.

Conclusion

In light of the foregoing, reconsideration and allowance of the claims is hereby earnestly requested.

Invitation for a Telephone Interview

The Examiner is requested to call the undersigned at (303) 740-1980 if there remains any issue with allowance of the case.

Request for an Extension of Time

Applicants respectfully petition for an extension of time to respond to the outstanding Office Action pursuant to 37 C.F.R. § 1.136(a) should one be necessary. Please charge our Deposit Account No. 02-2666 to cover the necessary fee under 37 C.F.R. § 1.17(a) for such an extension.

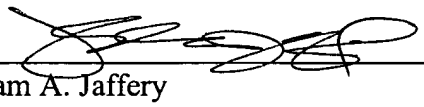
Charge our Deposit Account

Please charge any shortage to our Deposit Account No. 02-2666.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP

Date: June 22, 2005



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